

**LISTING OF CLAIMS**

1. (Currently Amended) A single bit FIR filter comprising:

a shift register comprising an input adapted to receive a plurality of serial input bits, said input bits being a single bit wide; said shift register input comprising a predetermined number of input nodes; said input nodes separated into at least two one or more sets of input nodes; wherein said input adapted to allow said plurality of input bits to shift down at the length of said shift register input;

    a storage device having a plurality of memory locations, each said memory location having an address;

means for using such that bits in a first set of input nodes can be utilized to address one of said memory locations and receive first content;

means for using bits in a second set of nodes, after applying an address offset to the bits which is not applied against the bits in the first set of nodes, to address one of said memory locations and receive second content; and

    an accumulator output providing at an output an accumulation of the first and second contents of said the memory locations that were addressed.

Claims 2-4. (Canceled).

5. (Currently Amended) A single bit FIR filter for comprising:  
a register having an input portion for receiving a stream of serial input bits, said register input portion comprising a plurality of input node sets, each said input node set outputting a set of is for receiving input bits from said serial stream of input bits;  
a memory comprising a plurality of memory locations each having an address and storing a value;  
first circuitry for addressing the , said memory locations addressed by bits of a first adapted to be addressed indirectly or directly by the contents at least one of said input node sets to retrieve a first value and second circuitry for addressing the memory locations addressed by bits of a second one of said node sets, following application of an address offset to those bits of the second node set which has not been applied against the bits of the first node set, to retrieve a second value;  
an accumulator adapted to receive the first and second values contents of said addressed memory locations; said accumulator adding said first and second values contents of said addressed memory locations and producing a result; said result being substantially an output of said single bit FIR filter.

6. (Canceled).

7. (Currently Amended) The single bit FIR filter of claim 5, wherein each input node set comprises a the same number of bits input nodes.

8. (Currently Amended) The single bit FIR filter of claim 5, wherein said input node sets comprise shift registers.

9. (Currently Amended) A method for providing a single bit FIR filter comprising: receiving serial data into a register an input, said register input being divided into first and second sets of input data locations;

using data from said first each set of input data locations to directly or indirectly address first memory locations associated with each set of input data;

applying an address offset to data from said second set of data locations to produce offset data, wherein the address offset is not applied against the data of the first set of data locations;

using the offset data to address second memory locations;

reading the contents of said addressed first and second memory locations;

accumulating the contents of said addressed first and second memory locations; and

providing a single bit FIR filter output comprising the accumulated contents.

10. (Currently Amended) The method of claim 9 further comprising, after said using step, shifting said input data in the register at least one input data position.

11. (Currently Amended) The method of claim 9 further comprising shifting said input data at least one input data position location in the register and after said step of providing repeating said method starting at said step of receiving.

12. (Original) The method of claim 9 further comprising loading said memory locations with values prior to the step of receiving.

13. (Currently Amended) The method of claim 9, wherein each set of input data locations comprises the same number of input bits.

14. (Currently Amended) A method of providing a single bit FIR filter comprising:  
inputting a ~~first bit of a~~ serial stream of data into register having a plurality of data locations an input portion;  
dividing said plurality of data locations input portion into first and second sets of data locations that can be used to address a memory directly or indirectly;  
addressing a memory location of a said memory with at least one set of data from the first set of data locations;  
applying an address offset to data from said second set of data locations to produce offset data, wherein the address offset is not applied against the data of the first set of data locations;  
addressing a memory location of the memory with the offset data;  
reading the contents of each addressed said memory location;  
accumulating the read contents from the addressed of said memory location with the contents of other memory locations; and  
providing the accumulated contents an output of said accumulator as an FIR output.

Claims 15-17. (Canceled)